Enrollment No: _____ Exam Seat No:_____

C.U.SHAH UNIVERSITY

Winter Examination-2015

Subject Name : Computer Organization and Architecture

Subject Code : 4TE04COA1 Branch: B.Tech (Computer Engineering)

Semester : IV Date : 20/11/2015 Time : 2.30 To 5.30 Marks : 70

Instructions:

(1) Use of Programmable calculator & any other electronic instrument is prohibited.
(2) Instructions written on main answer book are strictly to be obeyed.
(3) Draw neat diagrams and figures (if necessary) at right places.
(4) Assume suitable data if needed.

Q-1 **Attempt the following questions:**

a) Define following terms : **(08)**
i) computer organization, ii) computer Architecture, iii) Instruction cycle, iv) Machine cycle, v) Register Transfer Language, vi) Assembler, vii) Interrupt, viii) Micro operation **(01)**

b) The return address from the interrupt-service routine is stored on _____.
a) System heap
b) Processor register **(01)**
c) Processor stack
d) Memory

c) The addressing mode which makes use of in-direction pointers is _____.
a) Indirect addressing mode
b) Index addressing mode **(01)**
c) Relative addressing mode
d) Offset addressing mode

d) An 24 bit address generates an address space of _____ locations.
a) 1024
b) 4096 **(01)**
c) 2 ^ 48
d) 16,777,216

e) The addressing mode, where you directly specify the operand value is _____.
a) Immediate
b) Direct **(01)**
c) Definite
d) Relative

f) Which interrupt is unmaskable?
a) RST 5.5
b) RST 7.5 **(01)**
c) TRAP
d) Both a and b

g) The purpose of the ORIGIN directive is,
a) To indicate the starting position in memory, where the program block is to be stored
b) To indicate the starting of the computation code
c) To indicate the purpose of the code
d) To list the locations of all the registers used **(01)**

Attempt any four questions from Q-2 to Q-8

Q-2		**Attempt all questions**	**(14)**
	(a)	Explain instruction cycle with flow chart.	
	(b)	Explain general register organization.	
Q-3		**Attempt all questions**	
	(a)	Explain Memory-Reference Instructions.	**(05)**
	(b)	Explain MRI and Non-MRI with Example.	**(05)**
	(c)	Draw and explain 4-bit Binary adder-subtractor.	**(04)**
Q-4		**Attempt all questions**	**(14)**
	(a)	Explain stack with its respective operations.	
	(b)	Design and Explain common bus system with multiplexer.	
Q-5		**Attempt all questions**	**(14)**
	(a)	Explain overlapped register windows.	
	(b)	Explain Booth algorithm for multiplication operation.	
Q-6		**Attempt all questions**	
	(a)	Explain computer hardware configuration.	**(05)**
	(b)	Compare RISC Vs. CISC	**(05)**
	(c)	Explain Four-segment CPU pipeline.	**(05)**
Q-7		**Attempt all questions**	**(14)**
	(a)	Draw and explain flow chart of first pass assembler.	
	(b)	Explain the design of accumulator logic.	
Q-8		**Attempt all questions**	
	(a)	Write short note on vector processing.	**(05)**
	(b)	Write short note on parallel processing.	**(05)**
	(c)	Write short note on Instruction pipelining.	**(04)**